FIG. 1

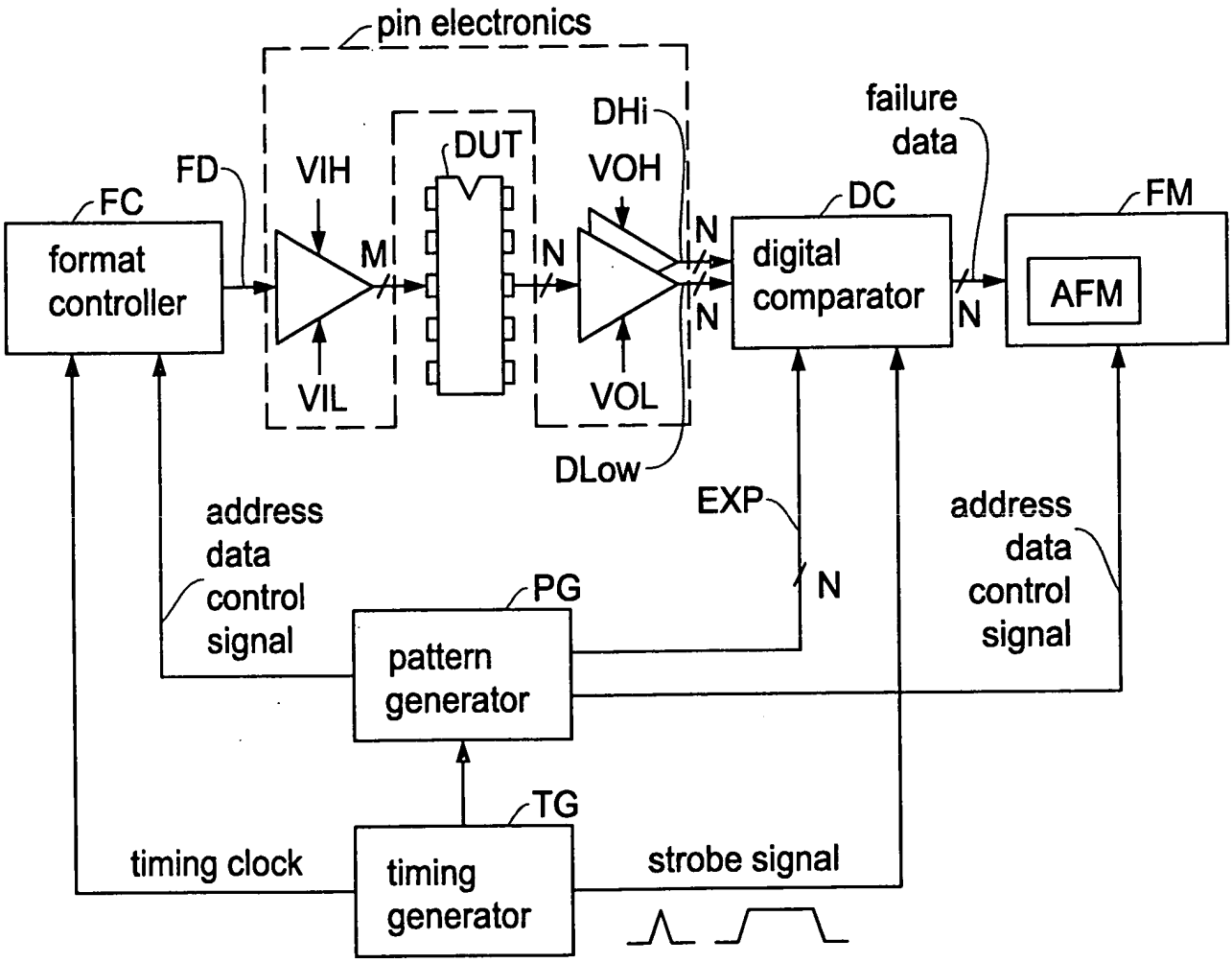

pin electronics
DHi
failure
data
DUT
FD
VIH
VOH
DC
FM
FC
format
controller
M
N
N
digital
comparator
AFM
N
N
VIL
VOL
DLow
EXP
address
data
control
signal
PG
N
address
data
control
signal
pattern
generator
TG
timing clock
timing
generator
strobe signal

FIG. 2A

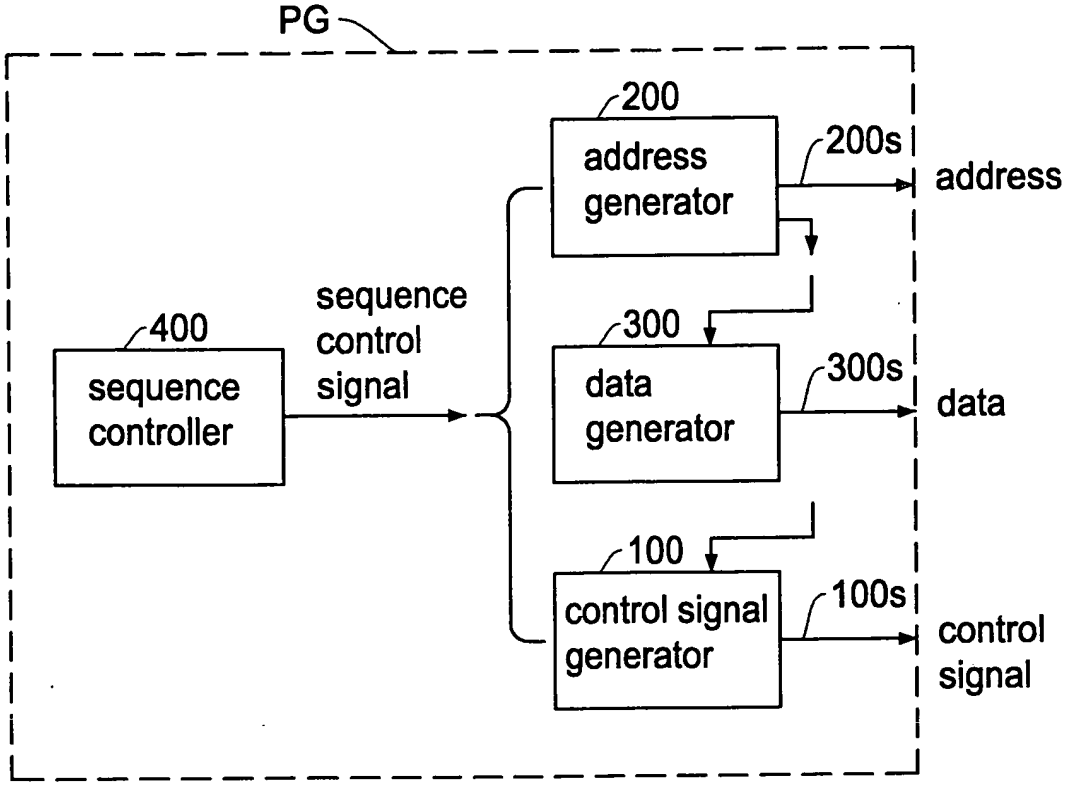

PG
200
address generator
200s
address
400
sequence controller
sequence control signal
300
data generator
300s
data
100
control signal generator
100s
control signal

FIG. 2B

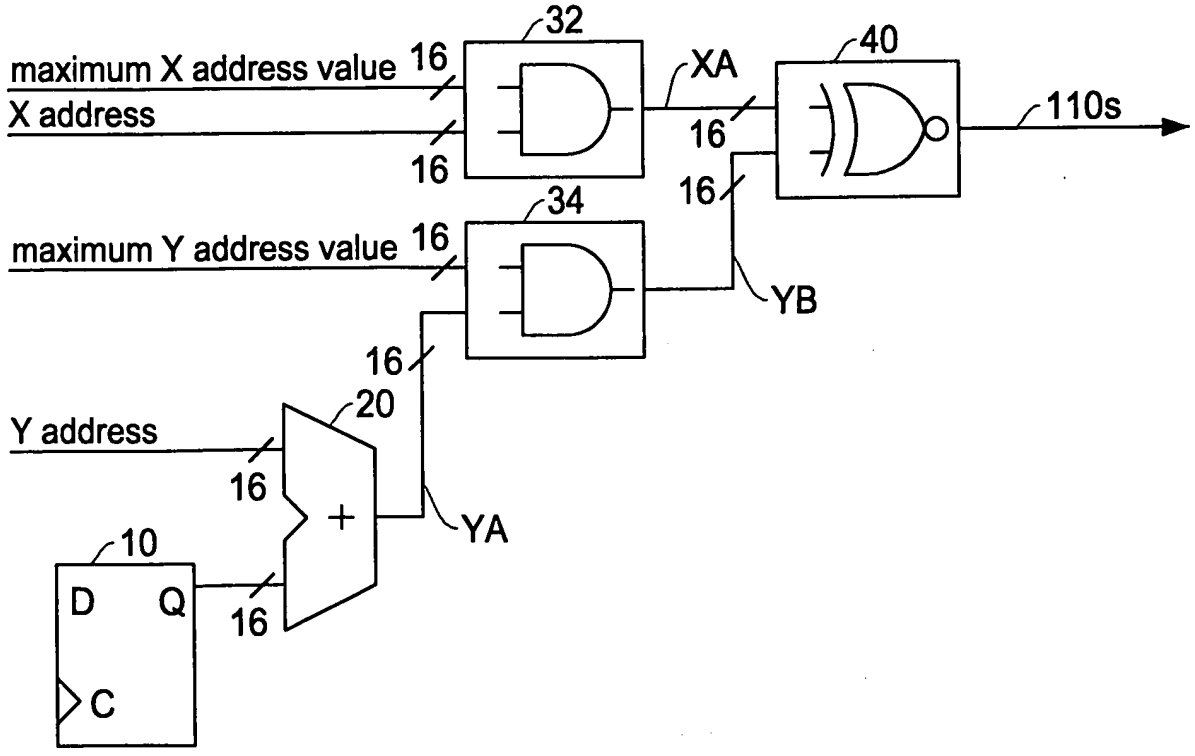

maximum X address value
16
X address
16
32
XA
16
40
110s
16
maximum Y address value
16
34
YB
16
20
Y address
16
+
YA
10
D
Q
16
C

FIG. 3A

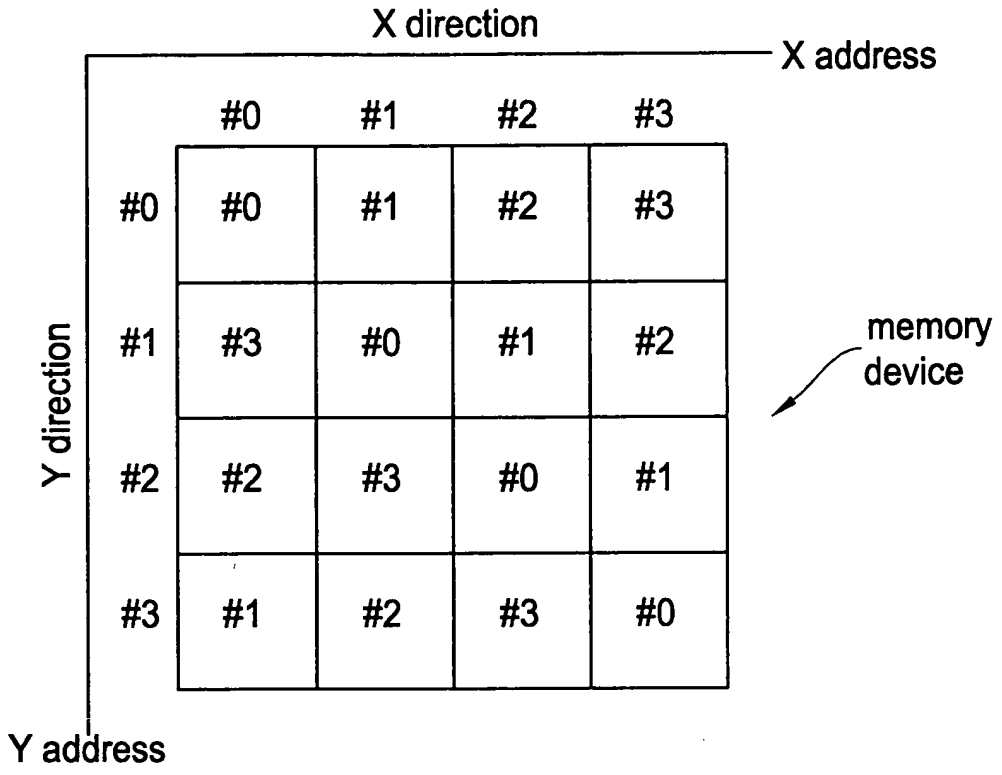

X direction
X address
#0 #1 #2 #3
#0 #0 #1 #2 #3
#1 #3 #0 #1 #2
#2 #2 #3 #0 #1
#3 #1 #2 #3 #0
Y direction
Y address
memory device

FIG. 3B

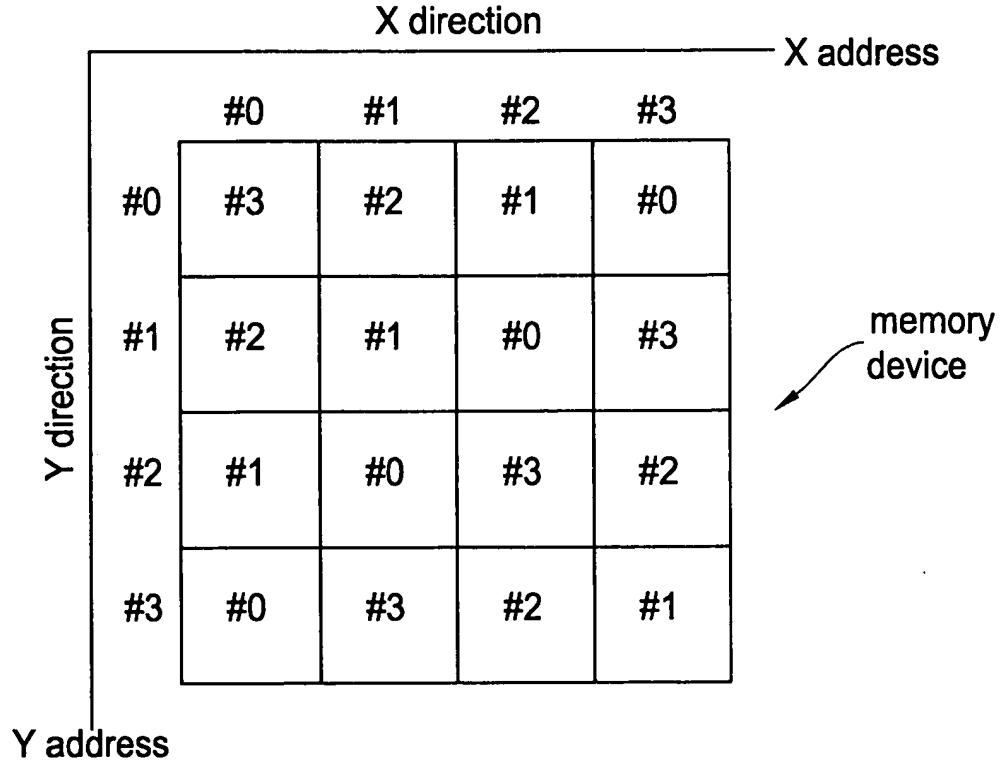

X direction
X address
#0 #1 #2 #3
#0 #3 #2 #1 #0
#1 #2 #1 #0 #3
#2 #1 #0 #3 #2
#3 #0 #3 #2 #1
Y direction
Y address
memory device

FIG. 4

max. X address value = #3
max. Y address value = #3
diagonal inversion set value = #3

X address of memory cell	#0	#1	#2	#3
X address of memory cell & maximum X address value	#0	#1	#2	#3

Y address of memory cell	Y address of memory cell + diagonal inversion set value & maximum Y address value
#0	#3
#1	#0
#2	#1
#3	#2

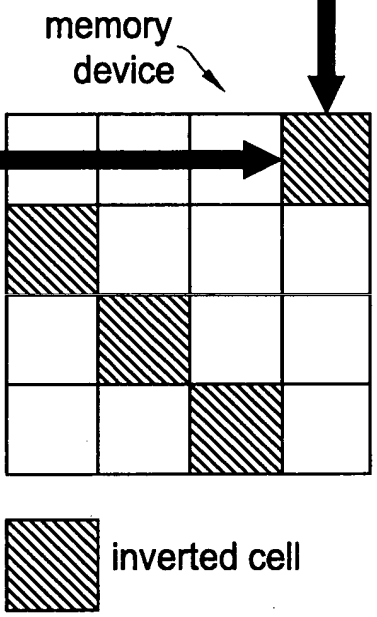


FIG. 5

max. X address value = #7
max. Y address value = #3
diagonal inversion set value = #3

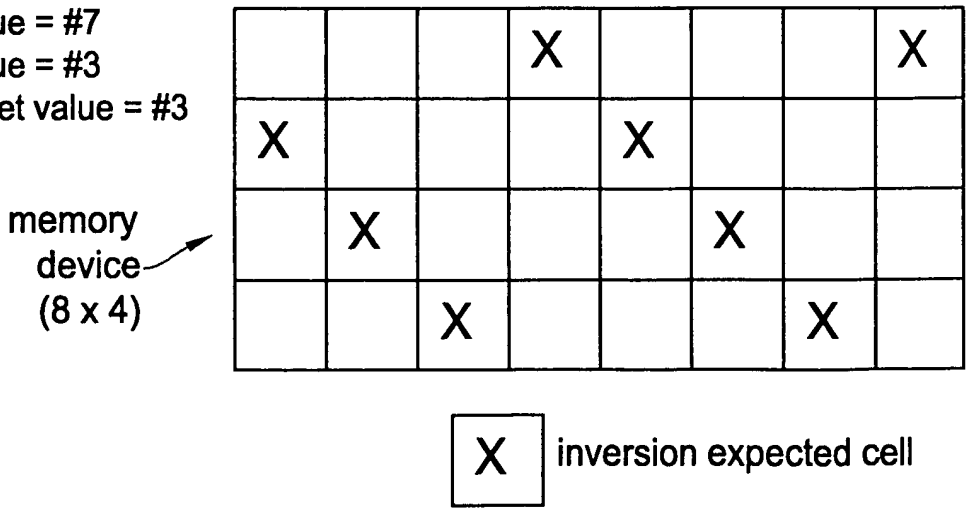
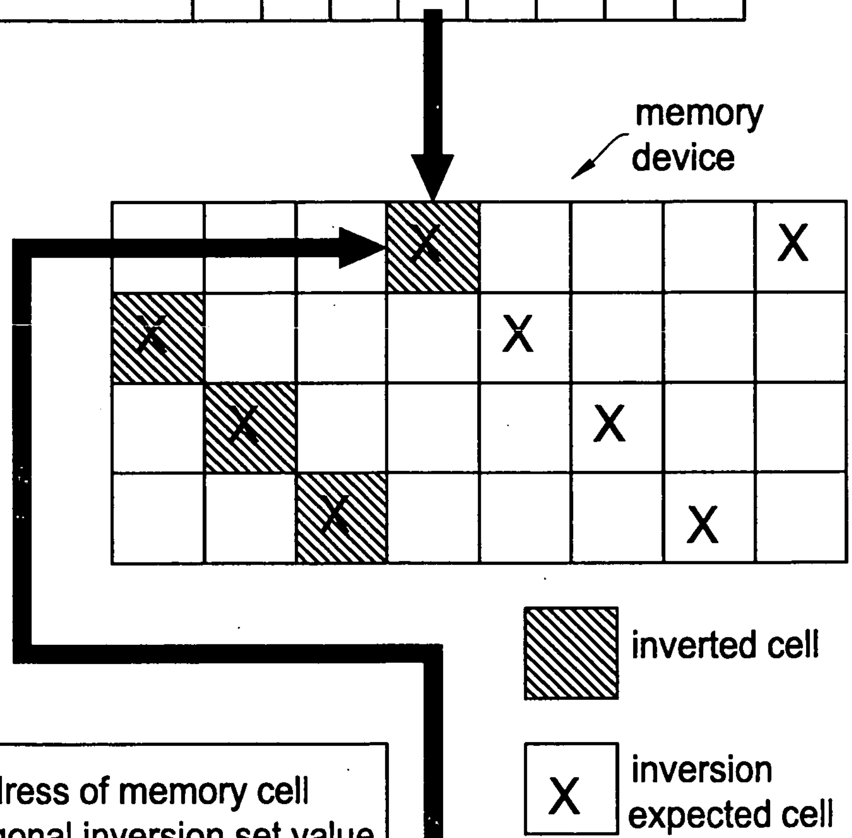


FIG. 6

max. X address value = #7
max. Y address value = #3
diagonal inversion set value = #3

X address of memory cell	#0	#1	#2	#3	#4	#5	#6	#7
X address of memory cell & maximum X address value	#0	#1	#2	#3	#4	#5	#6	#7



Y address of memory cell	Y address of memory cell + diagonal inversion set value & maximum Y address value
#0	#3
#1	#0
#2	#1
#3	#2

FIG. 7

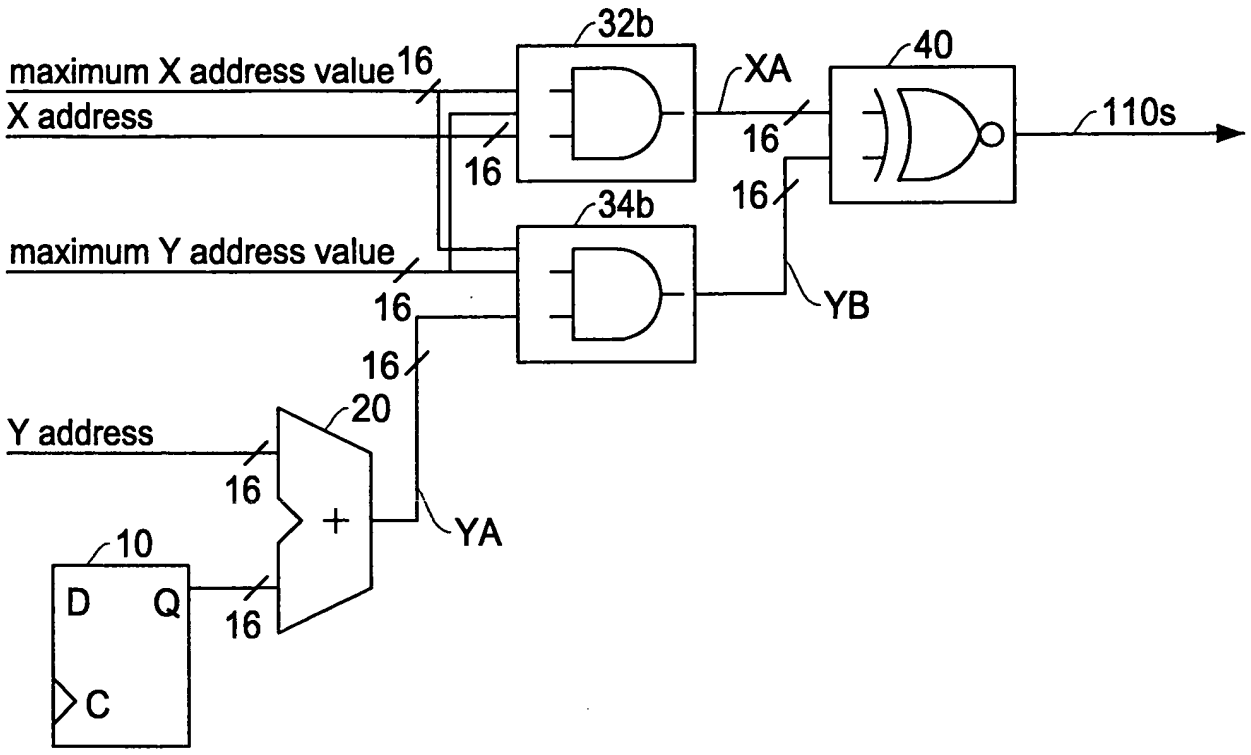
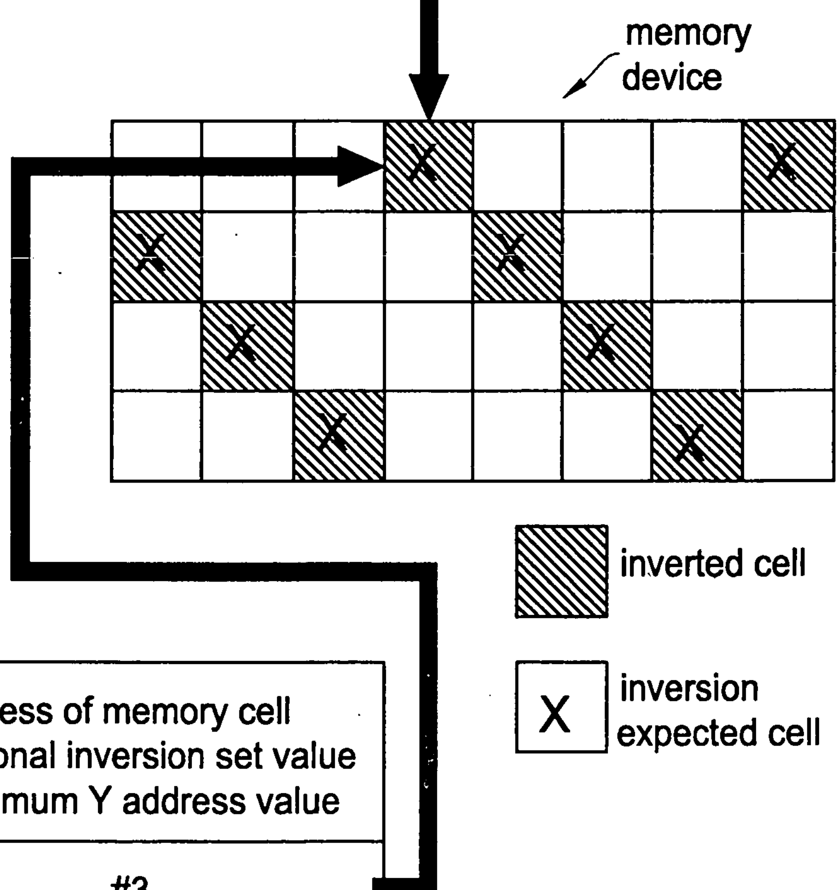

maximum X address value
16
X address
16
32b
XA
16
40
110s
16
maximum Y address value
34b
16
YB
16
Y address
20
16
+
YA
10
D
Q
16
C

FIG. 8

max. X address value = #7
max. Y address value = #3
diagonal inversion set value = #3

X address of memory cell	#0	#1	#2	#3	#4	#5	#6	#7
X address of memory cell & maximum X address value	#0	#1	#2	#3	#0	#1	#2	#3



Y address of memory cell	Y address of memory cell + diagonal inversion set value & maximum Y address value
#0	#3
#1	#0
#2	#1
#3	#2